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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/524,901	03/14/2000	Jieming Qi	AUS990869US1	8654

7590 03/03/2004

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EXAMINER	
CHANG, DANIEL D	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 03/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/524,901	QI ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7 and 11-17* is/are rejected.

7)☒ Claim(s) *2,3 and 8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 March 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(i) & 37 CFR 1.84(p) because lines, numbers & letters are not uniformly thick and well defined, clean, durable, and black (poor line quality). Also, some characters are too small.

Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 5 is objected to because of the following typographical errors: on line 2, "circuits" should be deleted; and on line 13, the word, "of" between "select" and "one" should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5, 6, 11, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamashita et al. (US 6,124,736).

Regarding claim 1, Yamashita discloses, in Fig. 3, a high speed static multiplexer (C102) comprising:

a plurality of data inputs (I0, I1) and at least one select input (S);

an output (O');

a high voltage rail (VDD) and a low voltage rail (GND);

a pull-up circuit (T120, T121, T124, T125) coupled between said output (O') and said high voltage rail (VDD) and further coupled to said plurality of data inputs (I0=1, I1=0) and said at least one select input (S), wherein said pull-up circuit generates a first logic state (O'=1) at said output in response to a selected data input (S=1) having said first logic state; and

a pull-down circuit (T122, T123, T126, T127) coupled between said output (O') and said low voltage rail (GND) and further coupled to receive said plurality of data inputs (I0=1, I1=0) and said at least one select input (S), wherein said pull-down circuit generates a second logic state (O'=0) at said output in response to a selected data input (S=0) having said second logic state.

Regarding claim 5, Yamashita discloses, in Fig. 3, a high-speed static multiplexer (C102) comprising:

at least two data inputs (I0, I1) that each receive a respective data input;

at least one select input (S), wherein each of said at least one select input receives a respective select signal;

an output (O'); and

a plurality of transistors (T120-T129) operationally coupled between said at least two data input circuits (I0, I1) and said output (O'), wherein said plurality of transistors each have a

control node (GATE) and a first and second data node (SOURCE/DRAIN) and wherein said plurality of transistors are controlled by both data inputs (I0, I1) and select signals (S=0, 1) to select of one of said data inputs to yield said output.

Regarding claim 6, Yamashita discloses, in Fig. 3, that the plurality of transistors include a P-type transistor (any one of T120, T121, T124, T125) and a plurality of sets of first (T122, T123), second (T126, T127), and third N-type transistors (T123, T127) for each of said at least two data inputs (I0, I1).

Regarding claim 11, Yamashita discloses, in Fig. 3, that the P-type transistor has an on state and off state (inherent) and wherein a voltage differential at said control node to change between said on and off states is less than the voltage differential between a high voltage applied at a second data node of said P-type transistor and a low voltage applied at a second data node of said third N-type transistor (transition signal of I0/I1 is less than VDD).

Regarding claim 12, Yamashita discloses, in Fig. 3, that the plurality of transistors are field effect transistors (FETs) (col. 12, lines 30+).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 7, 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. (US 6,124,736) in view of El Ayat et al. (US 5,698,992).

The teachings of Yamashita have been discussed above.

Regarding claim 13, Yamashita does not teach a multiplicative-input multiplexer having multiple levels.

However, El Ayat teaches a multiplicative-input multiplexer (Figs. 3F, 3G) having multiple levels for the purpose of providing large number of inputs.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have substituted the multiplexers of Yamashita with the multiplicative-input multiplexer as taught by El Ayat in order to provide more inputs.

Regarding claim 14, El Ayat discloses, in Fig. 3F, that the plurality of levels includes more than two levels (1^{st} level=362, 364, 368, 368; 2^{nd} level=396, 398; 3^{rd} level=410) with a final level having a single high speed static multiplexer (410), and wherein each of said outputs (386, 388, 390, 392, 400, 402) of a given level is fed into at least one input at a next level until said final level.

Regarding claim 15, since multiplexer of Yamashita is an inverted multiplexer (see O'), the modified multiplicative-input multiplexer will have an non-inverted output at each even number of level and an inverted output at each odd number of level.

Regarding claims 4, 7, 16, and 17, it is well known in the art that an inverter inverts a signal. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have provided the circuit of Yamashita or modified Yamashita with an inverter at the input or at the output in order to provide an inversion signal. It is an obvious matter of design choice.

Allowable Subject Matter

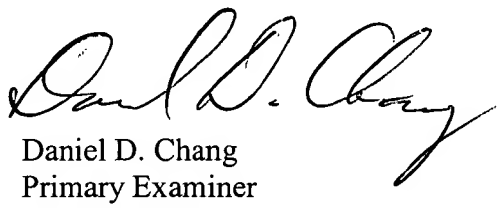
Claims 2, 3, and 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang
Primary Examiner
Art Unit 2819

DC

DANIEL CHANG
PRIMARY EXAMINER